APPLICATION NOTE

AN124

External synchronization for the NE5561/5568

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Synchronization of the 5561 can be accomplished by forcing the timing pin (Pin 5) above the 5.6V sawtooth limit comparator for a short time.

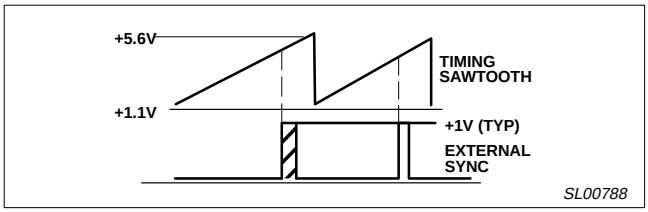

Figure 1.

This can be accomplished with a simple diode-coupled narrow pulse source with fairly low source impedance:

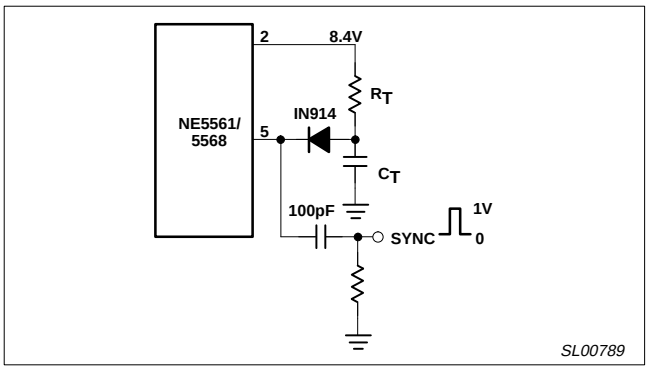

Figure 2.

A drawback to this approach is that when the 5.6V threshold is reached, a discharge transistor is turned on to quickly pull the timing capacitor to ground and will also attempt to pull the pulse generator to ground. This condition can be avoided by keeping the pulse width very narrow (0.1µs) or by placing a differentiator network between the pulse generator and the diode.

The differentiator will now produce a positive-going spike with the positive edge of the sync pulse, resetting the sawtooth without passing too much current through the discharge transistor. The negative spike produced by the falling edge of the clock will be blocked by the diode and will have no effect on the sawtooth ramp. A narrow sync pulse is no longer necessary while a sharp-edged pulse is. The value of C_D should be sufficient to ensure that a 10V pulse will drive the capacitor, C_T, high enough to trip the 5.6V comparator according to:

$$C_T \Delta V_{CT} = C_D(\Delta V_{CT} - V_D)$$

This relates the magnitude of the spike to the size of the pulse. Also assume $R_D C_D < 1\mu s$.

The free-running frequency of the slaved 5561 should be slightly lower than the sync frequency for proper operation.